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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,646	01/27/2004	Heon Lee	200300380-1	4583

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EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,646	LEE, HEON	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Applicants' Response to Office Action of Sept. 19, 2005 refers to newly submitted Drawings (Amendment to the Drawings, page 6), filed Dec. 21, 2005. However, because the Drawings appear to be missing from the file, Applicant is request to resubmit.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2, 4-5, 10-11, and 13-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mehregany et al. (U.S. Patent No. 6,136,243), in view of Chou (U.S. Patent No. 6,309,580), in further view of Chang (U.S. Patent Appl. Pub. No. 2002/0137331), in further view of Applicant's admitted Prior Art.

5. As to claim 1, Mehregany a discloses method of fabricating a silicon carbide structure (column 2, lines 5-7), comprising: patterning a mold layer (200) (column 4, lines 56-64); etching the mold layer (200) to form a cavity (204) in the mold layer (200); depositing a material comprising silicon carbide in the cavity to form a feature positioned in the cavity and a foundation layer connected with the feature (column 5, lines 18-24; Figure 1A); planarizing the foundation layer to form a substantially planar surface (column 5, lines 24-30); and extracting the silicon carbide imprint stamp by releasing the feature and the foundation layer from the mold layer (column 5, lines 30-34). Because Mehregany discloses forming cavity (204) with a standard photolithographic process (column 4, lines 61-63), there is a strong presumption that that first feature size that is greater than or equal to a lithography limit (Figure 2B).

6. Mehregany does not expressly disclose that the silicon carbide structure is an imprint stamp. Chou teaches a method of imprint lithography, including use of a molding layer (14) (column 7, lines 50-51; Figure 1A) (or imprint stamp) formed from silicon carbide (column 6, lines 59-66) using vapor deposition molding (column 7, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an imprint stamp using

Mehregany's method, because Chou teaches that imprint stamps are formed of silicon carbide using vapor deposition molding.

7. Mehregany does not expressly disclose a patterning consisting of a single masking step; and the etching consisting of a single etch step. Mehregany discloses that mask (202) (column 4, lines 59-61; Figure 2B) is used to etch the mold to depth (204) (column 4, lines 61-62) using a primary etch (column 5, lines 3-9; Figure 2C). Similarly, mask (206) is used to etch the mold to depth (208) using a secondary etch (column 5, lines 8-13; Figure 2D). However, case law has held that the omission of an element and its function is obvious if the function of the element is not desired. See MPEP § 2144.04(II)(A). Thus, if etching to a single depth is desired, the steps of patterning consisting of a single masking step; and the etching consisting of a single etching step are obvious.

8. In addition, Mehregany does not expressly disclose depositing a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity; and forming a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit. However, Mehregany's method is directed at forming molds in silicon substrates (column 3, lines 51-54), including the use of masking layers, dry etching, and lithography techniques (column 1, lines 12-16). Chang discloses a method of forming cavities with a reduced dimension (paragraph 0002) in silicon (paragraph 0003), including depositing a spacer layer (130) on the substrate layer (120), the spacer layer

conformally covering a surface of the cavity (150) (paragraph 0028; Figure 7); and forming a spacer (140A/140B) in the cavity (150) by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity (150) and the spacer partially fills the cavity (150) (paragraph 0028; Figure 8) so that the cavity includes a second feature size that is less than the lithography limit (paragraph 0029). Moreover, Chang's method produces features with dimensions that are not limited by the resolution of lithographic techniques (paragraph 0029). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity; and form a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit. Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a material comprising silicon carbide on the spacer and at least a portion of the feature includes the second feature size. One who is skilled in the art would be motivated to form features in silicon that are less than the resolution achieved by lithographic techniques.

9. In addition, Mehregany does not expressly disclose bonding a handling substrate with the foundation layer by applying heat and pressure to the handling substrate and the mold layer until the handling substrate and the foundation layer form a mechanical bond with each other. However, Applicant's admitted Prior Art

discloses a method of forming an imprint stamp (200), including bonding handling substrate (207) with the foundation layer (203) by applying heat and pressure to the handling substrate and the mold layer until the handling substrate and the foundation layer form a mechanical bond with each other (Specification, page 2, paragraph 2; Figures 3A-3B, 4A-4B). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to bond a handling substrate with the foundation layer by applying heat and pressure to the handling substrate and the mold layer until the handling substrate and the foundation layer form a mechanical bond with each other, because Applicant teaches that this method is useful in forming an imprint stamp.

10. As to claim 2, Applicant's admitted Prior Art discloses that the releasing comprises a grinding a backside surface of the mold layer (201) until the mold layer is released from the feature (203F) and the foundation layer (203) (Specification, page 2 paragraph 3; Figures 5A-5B).

11. As to claim 4, Applicant's admitted Prior Art discloses etching a remainder of the mold layer to effectuate the releasing of the feature and the foundation layer (Specification, page 2 paragraph 3; Figures 5A-5B). In addition, Mehregany discloses etching a remainder of the mold layer to effectuate the releasing of the feature and the foundation layer (column 5, lines 25-34). Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch the spacer layer in order to achieve a feature smaller than the resolution of lithography.

12. As to claim 5, Mehregany discloses that the surface of the cavity (204) includes a bottom surface and a sidewall surface (Figure 2C-2D). Chang discloses that the surface of the cavity (150) includes a bottom surface and a sidewall surface and the spacer (140A/140B) is connected with the sidewall surface of the cavity (paragraph 0028; Figure 8).

13. As to claim 10, Mehregany a discloses method of fabricating a silicon carbide structure (column 2, lines 5-7), comprising: patterning a mold layer (200) (column 4, lines 56-64); etching the mold layer (200) to form a cavity (204) in the mold layer (200); depositing a material comprising silicon carbide in the cavity to form a feature positioned in the cavity and a foundation layer connected with the feature and at least a portion of the feature includes the second feature size (column 5, lines 18-24; Figure 1A); planarizing the foundation layer to form a substantially planar surface (column 5, lines 24-30); and extracting the silicon carbide imprint stamp by releasing the feature and the foundation layer from the mold layer (column 5, lines 30-34). Because Mehregany discloses forming cavity (204) with a standard photolithographic process (column 4, lines 61-63), there is a strong presumption that that first feature size that is greater than or equal to a lithography limit (Figure 2B).

14. Mehregany does not expressly disclose that the silicon carbide structure is an imprint stamp. Chou teaches a method of imprint lithography, including use of a molding layer (14) (column 7, lines 50-51; Figure 1A) (or imprint stamp) formed from silicon carbide (column 6, lines 59-66) using vapor deposition molding (column 7, lines 1-5). Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to form an imprint stamp using Mehregany's method, because Chou teaches that imprint stamps are formed of silicon carbide using vapor deposition molding.

15. Mehregany does not expressly disclose a patterning consisting of a single masking step; and the etching consisting of a single etch step. Mehregany discloses that mask (202) (column 4, lines 59-61; Figure 2B) is used to etch the mold to depth (204) (column 4, lines 61-62) using a primary etch (column 5, lines 3-9; Figure 2C). Similarly, mask (206) is used to etch the mold to depth (208) using a secondary etch (column 5, lines 8-13; Figure 2D). However, case law has held that the omission of an element and its function is obvious if the function of the element is not desired. See MPEP § 2144.04(II)(A). Thus, if etching to a single depth is desired, the steps of patterning consisting of a single masking step; and the etching consisting of a single etching step are obvious.

16. In addition, Mehregany does not expressly disclose depositing a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity; and forming a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit. However, Mehregany's method is directed at forming molds in silicon substrates (column 3, lines 51-54), including the use of masking layers, dry etching, and lithography techniques (column 1, lines 12-16). Chang discloses a method of forming cavities with a reduced dimension (paragraph 0002) in silicon (paragraph 0003), including

depositing a spacer layer (130) on the substrate layer (120), the spacer layer conformally covering a surface of the cavity (150) (paragraph 0028; Figure 7); and forming a spacer (140A/140B) in the cavity (150) by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity (150) and the spacer partially fills the cavity (150) (paragraph 0028; Figure 8) so that the cavity includes a second feature size that is less than the lithography limit (paragraph 0029). Moreover, Chang's method produces features with dimensions that are not limited by the resolution of lithographic techniques (paragraph 0029). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity; and form a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit. Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a material comprising silicon carbide on the spacer and at least a portion of the feature includes the second feature size. One who is skilled in the art would be motivated to form features in silicon that are less than the resolution achieved by lithographic techniques.

17. In addition, Mehregany does not expressly disclose depositing a glue layer on the substantially planar surface of the foundation layer; and bonding a handling substrate with the glue layer by applying pressure and heat to the

handling substrate and the mold layer until the glue layer forms a mechanical bond with the foundation layer and the handling substrate. However, Applicant's admitted Prior Art discloses a method of forming an imprint stamp (200), including depositing a glue layer (205) on the substantially planar surface (203S) of the foundation layer (203); bonding a handling substrate (207) with the glue layer by applying pressure and heat to the handling substrate and the mold layer until the glue layer forms a mechanical bond with the foundation layer and the handling substrate (Specification, page 2, paragraph 2; Figures 3A-3B, 4A-4B). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a glue layer on the substantially planar surface of the foundation layer; and bond a handling substrate with the glue layer by applying pressure and heat to the handling substrate and the mold layer until the glue layer forms a mechanical bond with the foundation layer and the handling substrate, because Applicant teaches that this method is useful in forming an imprint stamp.

18. As to claim 11, Applicant's admitted Prior Art discloses that the releasing comprises a grinding a backside surface of the mold layer (201) until the mold layer is released from the feature (203F) and the foundation layer (203) (Specification, page 2 paragraph 3; Figures 5A-5B).

19. As to claim 13, Applicant's admitted Prior Art discloses etching a remainder of the mold layer to effectuate the releasing of the feature and the foundation layer (Specification, page 2 paragraph 3; Figures 5A-5B). In addition, Mehregany discloses etching a remainder of the mold layer to effectuate the

releasing of the feature and the foundation layer (column 5, lines 25-34). Moreover, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch the spacer layer in order to achieve a feature smaller than the resolution of lithography.

20. As to claim 14, Mehregany discloses that the surface of the cavity (204) includes a bottom surface and a sidewall surface (Figure 2C-2D). Chang discloses that the surface of the cavity (150) includes a bottom surface and a sidewall surface and the spacer (140A/140B) is connected with the sidewall surface of the cavity (paragraph 0028; Figure 8).

Claim Rejections - 35 USC § 103

21. Claims 3 and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mehregany, in view of Chou, in further view of Chang, in further view of Applicant's admitted Prior Art, in further view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002).

22. As to claims 3 and 12, Mehregany does not expressly disclose that the grinding comprises a chemical mechanical planarization process. Wolf teaches that chemical mechanical polishing (or chemical mechanical planarization) is a well-recognized planarization technology, appropriate for polishing both conductor and dielectric materials, and is capable of achieving planarization on a global scale (page 313). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a chemical mechanical planarization process. One who is skilled in the art would be

motivated to use a well-recognized planarization technology, appropriate for polishing both conductor and dielectric materials, and capable of achieving planarization on a global scale.

Claim Rejections - 35 USC § 103

23. Claims 6-7 and 15-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mehregany, in view of Chou, in further view of Chang, in further view of Applicant's admitted Prior Art, in further view of Jeong et al. (U.S. Patent No. 6,943,117).

24. As to claims 6 and 15, Mehregany does not expressly disclose that after the extracting, forming a master imprint stamp by mounting a plurality of the silicon carbide imprint stamps to a master substrate. However, Jeong discloses a method of imprint lithography (column 1, lines 10-14), including forming a master imprint stamp (40) by mounting a plurality of imprint stamps (41) to a master substrate (column 8, lines 45-59; Figure 6). Jeong teaches that it is more effective to imprint features on a large substrate with a features formed on single stamp as large as the substrate (column 2, lines 22-30) because only a single imprinting step is performed, which eliminates the need to repeated realign the stamp as in the step and repeat imprinting process (column 2, lines 14-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a master imprint stamp by mounting a plurality of the silicon carbide imprint stamps to a master substrate. One who is

skilled in the art would be motivated to more effectively imprint features on a large substrate.

25. As to claim 7 and 16, Mehregany does not expressly disclose positioning a plurality of the silicon carbide imprint stamps in an array of rows and columns on the master substrate. However, Jeong discloses a method of imprint lithography (column 1, lines 10-14), including positioning a plurality of imprint stamps in an array of rows and columns on the master substrate (column 10, lines 31-37; Figure 18). Jeong teaches that such an arrangement maximizes the utilization of a large substrate (column 10, lines 35-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to position a plurality of the silicon carbide imprint stamps in an array of rows and columns on the master substrate. One who is skilled in the art would be motivated to more effectively imprint features on a large substrate and to select an arrangement to maximize utilization of a large substrate.

Claim Rejections - 35 USC § 103

26. Claims 8-9 and 17-18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mehregany, in view of Chou, in further view of Chang, in further view of Applicant's admitted Prior Art, in further view of Rossnagel et al., *Handbook of Plasma Processing*, Noyes Publications (1990).

27. As to claims 8 and 17, Mehregany does not expressly disclose that the forming the spacer comprises a reactive ion etching of the spacer layer. Chang discloses that forming the spacer (140A/140B) comprises anisotropically etching

of the spacer layer (130) (paragraph 0028). Rossnagel teaches that reaction ion etching is anisotropic and is a commonly used etching method to form features in silicon (page 198-199). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacer comprising a reactive ion etching of the spacer layer. One who is skilled in the art would be motivated to use a conventional silicon etching method.

28. As to claims 9 and 18, Mehregany does not expressly disclose that the etching the mold layer comprises an anisotropic reactive ion etching of the mold layer to form the cavity. Rossnagel teaches that reaction ion etching is anisotropic and is a commonly used etching method to form features in silicon (page 198-199). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch the mold layer comprising an anisotropic reactive ion etching of the mold layer to form the cavity. One who is skilled in the art would be motivated to use a conventional silicon etching method.

Response to Arguments

29. Applicant's arguments (Applicant's Remarks, section (ii)(b), pages 8-11), filed Dec. 21, 2005, regarding the rejection of claims 1-2, 4-5, 10-11 and 13-14 under 35 U.S.C. 103(a) as being unpatentable over Mehergany, in view of Chou, in further view of Chang, have been fully considered but they are not persuasive.

30. First, Applicant argues that Mehregany teaches away from "the patterning consisting of a single masking step" and "the etching consisting of a single etch

step" (page 9). Mehregany discloses that mask (202) (column 4, lines 59-61; Figure 2B) is used to etch the mold to depth (204) (column 4, lines 61-62) using a primary etch (column 5, lines 3-9; Figure 2C). Similarly, mask (206) is used to etch the mold to depth (208) using a secondary etch (column 5, lines 8-13; Figure 2D). However, case law has held that the omission of an element and its function is obvious if the function of the element is not desired. See MPEP § 2144.04(II)(A). Thus, if etching to a single depth is desired, the steps of patterning consisting of a single masking step; and the etching consisting of a single etching step are obvious.

31. Second, Applicant argues that Mehregany is non-operative for use as an imprint stamp (pages 9-10). However, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Mehregany is a general teaching reference, which demonstrates that silicon carbide structures can be formed by depositing silicon carbide on silicon molds formed by etching (column 4, lines 56-67; column 5, lines 1-35). Chou teaches that imprint stamps are formed from silicon carbide (column 6, lines 59-66) using vapor deposition molding (column 7, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an imprint stamp using Mehregany's method, because Chou teaches that imprint stamps are formed of silicon carbide using vapor deposition molding. Applicant has not

provided any evidence (e.g., unexpected results) to rebut the *prima facie* case for obviousness.

32. Third, Applicant argues that the Chang reference includes several additional steps (forming the plug-like structure; depositing and etching the first oxide; and etching away of the plug-like structure) that are not recited in claims 1 and 10 (page 10). However, claims 1 and 10 use the transitional phrase "comprising." The transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See MPEP § 2111.03. Thus, Applicant's claims 1 and 10 do not exclude the several additional steps recited in the Chang reference.

33. Fourth, Applicant argues that Chou is silent as to how the imprint stamp is formed (page 11). However, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Mehregany is a general teaching reference, which demonstrates that silicon carbide structures can be formed by depositing silicon carbide on silicon molds formed by etching (column 4, lines 56-67; column 5, lines 1-35). Chou teaches that imprint stamps are formed from silicon carbide (column 6, lines 59-66) using vapor deposition molding (column 7, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an imprint stamp using Mehregany's method, because Chou teaches that imprint stamps

are formed of silicon carbide using vapor deposition molding. Applicant has not provided any evidence (e.g., unexpected results) to rebut the *prima facie* case for obviousness.

34. Lastly, Applicant argues that the Admitted Prior Art does not teach or suggest the deposition and etching of a spacer layer to reduce the feature sizes in the mold to sub-lithographic feature size (page 11). However, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). However, the Mehregany, Chou, and Change references teach or suggest the deposition and etching of a spacer layer to reduce the feature sizes in the mold to sub-lithographic feature size.

35. Applicant's arguments (Applicant's Remarks, section (ii)(b), page 12), filed Dec. 21, 2005, regarding the rejection of claims 2-9 and 11-18 under 35 U.S.C. 103(a) as being unpatentable have been fully considered but they are not persuasive, as discussed above.

36. Applicant's arguments (Applicant's Remarks, section (ii)(c), page 12), filed Dec. 21, 2005, regarding the rejection of claims 3 and 12 under 35 U.S.C. 103(a) as being unpatentable have been fully considered but they are not persuasive, as discussed above.

37. Applicant's arguments (Applicant's Remarks, section (ii)(d), page 12), filed Dec. 21, 2005, regarding the rejection of claims 6-7 and 15-16 under 35 U.S.C.

103(a) as being unpatentable have been fully considered but they are not persuasive, as discussed above.

38. Applicant's arguments (Applicant's Remarks, section (ii)(e), page 13), filed Dec. 21, 2005, regarding the rejection of claims 8-9 and 11-18 under 35 U.S.C. 103(a) as being unpatentable have been fully considered but they are not persuasive, as discussed above.

Conclusion

39. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
Feb. 13, 2006

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER